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| EXAMINER | |
|---|---|
| TRAN, MAI HUONG C | |
| ART UNIT | PAPER NUMBER |
| 2818 | |

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 10/042,090 | Applicant(s) STREET ET AL. | |
|---|---|---|---|
| | Examiner Mai-Huong Tran | Art Unit 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4)☐ Interview Summary (PTO-413) Paper No(s) _____
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other.

# DETAILED ACTION

## Specification

The specification is objected to for the following reasons.

The specification includes incorrect reference signs 'passivation walls 113' on page 14, lines 16 and 31. It must be 'passivation walls 210'. Correction is required.

## Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,054,746 to Bird et al.

Bird discloses an image sensor array comprising a plurality of pixels 2 arranged in rows and columns, each pixel including a contact pad 5 and pixel circuitry 22 connected to the contact pad 5; a passivation layer 12 defining a plurality of trenches 13, each trench being surrounded by passivation walls having upper edges, wherein the contact pad 5 of each pixel is located in an associated trench such that an upper surface of the contact pad is located below the upper edges of the passivation walls; a sensor layer formed over the

passivation layer and having lower portions extending into the trenches, wherein each lower portion of the sensor layer abuts the upper surface of an associated pixel contact pad as set forth in cols. 3-8 and figs. 1-5.

Regarding to claims 2 and 15, the image sensor array wherein the sensor layer is an amorphous silicon (a-Si:H) layer further comprising: an upper region that is doped with a p-type dopant; and an undoped central region that is located between the upper region and the lower portions, wherein the lower portions of the a-Si:H layer that are doped with an n-type dopant, and wherein the passivation walls extend into the central, relatively undoped region of the a-Si layer (cols. 3-8 and figs. 1-5).

Regarding to claim 3, the image sensor array, further comprising a conductor formed below each of the passivation walls, wherein the conductor is connected to a low voltage source such that the conductor generates a field that impedes the flow of electrons from a metal contact pad of a first pixel to a metal contact pad of a second pixel via the passivation wall (cols. 3-8 and figs. 1-5).

Regarding to claim 4, the image sensor array, wherein portions of selected conductors extend under the contact pad of associated pixels such that a capacitor is formed by each portion and the contact pad of the associated pixel (cols. 3-8 and figs. 1-5).

Regarding to claim 5, the image sensor array, wherein the sensor layer is an amorphous silicon (aSi:H) layer further comprising an upper region that is doped with a p-type dopant, and a central region that is located between the upper region and the lower portions, and wherein the central region and the lower portions of the a-Si:H layer are undoped (cols. 3-8 and figs. 1-5).

Regarding to claims 6 and 14, the image sensor array, wherein side surfaces of the passivation walls are sloped such that the lower portion of the a-Si:H layer forms an angle in the range of 45° and 60° relative to the upper surface of the contact pad (figs. 2 and 3).

Regarding to claim 7, the image sensor array, further comprising a conductor formed below each of the passivation walls, wherein the metal structure is connected to a low voltage source such that the metal structure generates a field that impedes the flow of electrons from a metal contact pad of a first pixel to a metal contact pad of a second pixel via the passivation wall (cols. 3-8 and figs. 1-5).

Regarding to claim 9, Bird discloses an image sensor array comprising a plurality of pixels 2 including a first pixel having a first contact pad 5 and a second pixel having a second contact pad that is separated from the first contact pad by an elongated interface region; a continuous sensor layer formed over the plurality of pixels and having lower

portions contacting the first and second contact pads, respectively; and a plurality of conductors 4 including a first conductor extending under the interface region separating the first and second contact pads, wherein the plurality of conductors 4 are connected to a low voltage source such that the first conductor generates a field that impedes the flow of electrons across the interface region from the first contact pad of the first pixel to the second contact pad of the second pixel (cols. 3-8 and figs. 1-5).

Regarding to claim 10, the image sensor array wherein the first conductor further comprises a portion extending under the first contact pad such that a capacitor is formed by the portion and the first contact pad (cols. 3-8 and figs. 1-5).

Regarding to claim 11, the image sensor array, further comprising a passivation layer including portions provided in the interface region separating the first and second contact pads (cols. 3-8 and figs. 1-5).

Regarding to claim 12, the image sensor, wherein the passivation layer defines a plurality of trenches and the portions of the passivation layer comprise passivation walls surrounding the trenches, each of the passivation walls having upper edges, and wherein the first contact pad is located in a first trench and the second contact pad is located in a second trench adjacent to the first trench such that a first passivation wall is located between the first contact pad and the second contact pad, and such that the upper surfaces

of the first and second contact pads are located below the upper edge of the first passivation wall (cols. 3-8 and figs. 1-5).

Regarding to claim 16, the image sensor array, wherein the continuous sensor layer is an amorphous silicon (a-Si:H) layer further comprising an upper region that is doped with a p-type dopant, and a central region that is located between the upper region and the lower portions, and wherein the central region and the lower portions of the a-Si:H layer are undoped (cols. 3-8 and figs. 1-5).

Regarding to claim 17, Bird discloses an image sensor array comprising a plurality of pixels 2 arranged in rows and columns, each pixel including a contact pad 5 and pixel circuitry 22 connected to the contact pad 5; and a continuous amorphous silicon layer formed over the plurality of pixels, the amorphous silicon layer including a continuous doped region and a continuous intrinsic region located under the doped region and contacting an upper surface of the contact pad of each of the plurality of pixels (cols. 3-8 and figs. 1-5).

Regarding to claim 18, the image sensor array, wherein the plurality of pixels include a first pixel having a first contact pad and a second pixel having a second contact pad separated from the first contact pad by an interface region, and wherein the sensor

array further comprises a passivation layer including portions provided in the interface region separating the first and second contact pads (cols. 3-8 and figs. 1-5).

Regarding to claim 19, the image sensor, wherein the passivation layer defines a plurality of trenches and the portions of the passivation layer comprise passivation walls surrounding the trenches, each of the passivation walls having upper edges, and wherein the first contact pad is located in a first trench and the second contact pad is located in a second trench adjacent to the first trench such that a first passivation wall is located between the first contact pad and the second contact pad, and such that the upper surfaces of the first and second contact pads are located below the upper edge of the first passivation wall (cols. 3-8 and figs. 1-5).

Regarding to claim 20, the image sensor, further comprising a plurality of conductors including a first conductor extending under the interface region separating the first and second contact pads, wherein the plurality of conductors are connected to a low voltage source such that the first conductor generates a field that impedes the flow of electrons across the interface region from the first contact pad of the first pixel to the second contact pad of the second pixel (cols. 3-8 and figs. 1-5).

## Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. patent No. 6,054,746 to Bird et al. in view of Cox et al. (5,043,582).

Bird discloses the claimed invention except for the passivation walls are formed from a material selected from the group consisting of $SiO_2$, SiON, and benzocyclobutene (BCB). Cox teaches the passivation walls are formed from a material selected from the group consisting of $SiO_2$, SiON, and benzocyclobutene (BCB) as set forth in col. 18, lines 59-62.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the passivation walls from a material selected from the group consisting of $SiO_2$, SiON, and benzocyclobutene (BCB), as taught by Cox in order to provide a solid state imaging system and detector which are highly sensitive to x-radiation and can produce highly accurate x-ray images (col. 1, lines 53-56).

**Conclusion**

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (703) 305-1958. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

HOAI HO
PRIMARY EXAMINER